

Appl. No. 10/707,703
Amdt. dated February 23, 2005
Reply to Office action of December 02, 2004

LISTING OF THE CLAIMS

1. (original) A high density read-only memory (ROM) cell
installed on a silicon substrate for storing data, comprising:
5 a first doped region being of a second conductive type
installed on the silicon substrate;
a plurality of first heavily doped regions being of a first
conductive type installed in the first doped region;
a second doped region being of the second conductive type
10 installed on the silicon substrate; and
a gate installed on the surface of the silicon substrate
and adjacent to the first doped region and the second
doped region.
- 15 2. (original) The ROM cell of claim 1 installed in a doped well
being of the first conductive type on the silicon substrate.
3. (original) The ROM cell of claim 1 wherein the first conductive
type is P-type, and the second conductive type is N-type.
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4. (original) The ROM cell of claim 1 wherein the first conductive
type is N-type, and the second conductive type is P-type.
5. (original) The ROM cell of claim 1 wherein the first doped
25 region is a drain doped region and the second doped region
is a source doped region, and each of the plurality of heavily
doped regions and the first doped region form a diode so that
a plurality of drain signals respectively passing through the
plurality of heavily doped regions do not interfere with each

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other.

6. (previously presented) A high density ROM cell installed on a silicon substrate for storing data, comprising:

- 5 a plurality of drain doped regions being of a second
conductive type installed on the silicon substrate;
a source doped region being of the second conductive type
installed on the silicon substrate; and
a gate installed on the surface of the silicon substrate
10 and adjacent to the plurality of drain doped regions
and the source doped region, the gate having at least
one extension structure respectively located between
one of the plurality of drain doped regions and another
drain doped region so that a plurality of drain signals
15 respectively passing through the plurality of drain
doped regions do not interfere with each other.

7. (previously presented) The ROM cell of claim 6 installed in a doped well being of a first conductive type on the silicon
20 substrate.

8. (original) The ROM cell of claim 7 wherein the first conductive type is P-type, and the second conductive type is N-type.

25 9. (original) The ROM cell of claim 7 wherein the first conductive type is N-type, and the second conductive type is P-type.

10. (original) The ROM cell of claim 6 wherein the second conductive type is N-type.

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11. (original) The ROM cell of claim 6 wherein the second
conductive type is P-type.

5 12. (cancelled)